

Appl. No. 09/517,345
Amdt. dated September 15, 2005
Amendment under 37 CFR 1.116 Expedited Procedure
Examining Group 2811

PATENT

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 1 1. (Previously Amended) An integrated circuit package comprising:
2 a silicon die having a first thickness;
3 a metallized polymer layer having a first side and a second side; and
4 a transition medium disposed between the silicon die and the first side of the
5 metallized polymer layer; and
6 a plastic encapsulant which encapsulates the silicon die and the transition
7 medium, the plastic encapsulant and transition medium each having a coefficient of thermal
8 expansion between approximately $7 \times 10^{-6}/^{\circ}\text{C}$ and $15 \times 10^{-6}/^{\circ}\text{C}$,
9 wherein the transition medium has a second thickness,
10 the first thickness of the silicon die is less than the second thickness,
11 a first edge of the transition medium is coincident with a first edge of the silicon
12 die, and
13 a second edge of the transition medium is coincident with a second edge of the
14 silicon die.
- 15 2. (Original) The integrated circuit package of claim 1 wherein the transition
16 medium is nonconductive.
- 17 3. (Cancelled)
- 18 4. (Previously Amended) The integrated circuit package of claim 1 wherein
19 the transition medium comprises a mold compound material.
- 20 5. (Cancelled)

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21 6. (Original) The integrated circuit package of claim 1 wherein the presence
22 of the transition medium reduces stress and fracture damage to the silicon die.

23 7. (Previously Amended) The integrated circuit package of claim 1 wherein a
24 thickness of the metallized polymer layer and a thickness of the plastic encapsulant define a
25 package thickness, wherein the silicon die is disposed at a location approximately equally spaced
26 from the bottom of the metallized polymer layer and the top of the plastic encapsulant.

27 8. (Original) The integrated circuit package of claim 7 wherein the package
28 thickness is approximately 0.060 inches or less.

29 9. (Previously Amended) The integrated circuit package of claim 1 wherein
30 the first thickness is less than approximately 6 mils.

31 10. (Original) The integrated circuit package of claim 1 wherein the silicon
32 die is coupled to the transition medium through an adhesive.

33 11. (Previously Presented) The integrated circuit package of claim 10 wherein
34 a coefficient of thermal expansion for the adhesive is approximately $58 \times 10^{-6}/^{\circ}\text{C}$.

35 12. (Previously Presented) The integrated circuit package of claim 1 wherein
36 the metallized polymer layer is a tape carrier having a dielectric layer and a conductive layer.

37 13. (Original) The integrated circuit package of claim 12 comprising solder
38 balls mounted to the second side of the metallized polymer layer, the solder balls electrically
39 contacting an etched circuit in a conductive layer of the tape carrier.

40 14. (Original) The integrated circuit package of claim 13 wherein the solder
41 balls electrically connect the integrated circuit package to a printed circuit board.

42 15. (Original) The integrated circuit package of claim 14 wherein the solder
43 balls are arranged in a grid fashion underneath the position for the silicon die.

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44 16. (Original) The integrated circuit package of claim 1 wherein the cross
45 sectional area of the silicon die is substantially less than or equal to the cross sectional area of the
46 rigid transition medium.

47 17. (Previously Presented) The integrated circuit package of claim 14 wherein
48 the silicon die has been lapped to the first thickness.

49 18. (Original) The integrated circuit package of claim 1 wherein the package
50 is a BGA package.

51 19. (Original) The integrated circuit package of claim 1 wherein a volume of
52 the silicon die is less than the volume of the rigid transition medium.

53 20. (Previously Presented) An integrated circuit package comprising:
54 a metallized polymer layer defining a first thickness;
55 at least one solder ball, the at least one solder ball and metallized polymer layer
56 comprise a flat surface;
57 a transition medium coupled to the metallized polymer layer;
58 a die coupled to the transition medium; and
59 a mold cap encapsulating the transition medium and the die, the mold cap
60 defining a second thickness,
61 wherein the first thickness and second thickness define a package thickness,
62 the transition medium and the mold cap each comprising a first mold compound,
63 and
64 the die is disposed near a midline of the package thickness measured from the
65 bottom of the metallized polymer layer to the top of the mold cap.

66 21. (Original) The integrated circuit package of claim 20 wherein the mold
67 cap has a coefficient of thermal expansion similar to a coefficient of thermal expansion of the
68 transition medium.

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69 22. (Original) The integrated circuit package of claim 20 wherein the die is
70 mounted to the transition medium with a layer of adhesive.

71 23. (Previously Presented) The integrated circuit package of claim 20 wherein
72 a first edge of the transition medium is coincident with a first edge of the die, a second edge of
73 the transition medium is coincident with a second edge of the die.

74 24. (Original) The integrated circuit package of claim 20 wherein the
75 metallized polymer layer is a tape carrier.

76 25. (Previously Presented) An integrated circuit package comprising:
77 a tape carrier defining a thickness;
78 a first adhesive layer disposed on the tape carrier, the first adhesive layer having a
79 coefficient of thermal expansion and a thickness;
80 a transition medium having a first surface and a second surface, wherein the first
81 surface of the transition medium engages the first adhesive layer, the transition medium having a
82 coefficient of thermal expansion and a thickness;
83 a second adhesive layer disposed on the second surface of the transition medium,
84 the second layer of adhesive having a coefficient of thermal expansion and a thickness;
85 a die disposed on the second adhesive layer comprising a thickness that is less
86 than the thickness of the transition medium, wherein a first edge of the transition medium is
87 coincident with a first edge of the die, and a second edge of the transition medium is coincident
88 with a second edge of the die; and
89 a mold cap encapsulating the first adhesive layer, the transition medium, the
90 second adhesive layer and the die, wherein the transition medium and the mold cap each
91 comprising a first mold compound, thereby the transition medium and the mold cap have
92 approximately the same coefficient of thermal expansion so as to reduce the thermal stress on the
93 die during thermal cycling.

94 26-48. (Cancelled)

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- 95 49. (Previously Presented) An integrated circuit package comprising:
96 an integrated circuit die having a front side, a back side, and a first thickness
97 between the front and back sides, wherein bonding pads are formed on the front side;
98 a metallized polymer layer having a first side and a second side, wherein the
99 bonding pads are electrically coupled to features of the metallized polymer layer; and
100 a transition medium comprising a mold compound, between the integrated circuit
101 die and the metallized polymer layer, wherein the transition medium has a second thickness,
102 greater than the first thickness, a first edge of the transition medium is coincident with a first
103 edge of the integrated circuit die, and a second edge of the transition medium is coincident with a
104 second edge of the integrated circuit die.
- 105 50. (Previously Presented) The integrated circuit package of claim 49 wherein
106 the front side of the integrated circuit die faces away from the metallized polymer layer.
- 107 51. (Previously Presented) The integrated circuit package of claim 49 wherein
108 the integrated circuit die, metallized polymer layer, and transition medium are three parallel
109 planes.
- 110 52. (Previously Presented) The integrated circuit package of claim 49 wherein
111 the transition medium has a single, relatively uniform thickness.
- 112 53. (Previously Presented) The integrated circuit package of claim 49 wherein
113 the integrated circuit package accommodates only a single integrated circuit die.
- 114 54. (Previously Presented) The integrated circuit package of claim 49 further
115 comprising:
116 bonding wires to electrically couple the bonding pads to the features of the
117 metallized polymer layer.
- 118 55. (Previously Presented) The integrated circuit package of claim 49 wherein
119 the transition medium does not comprise metal.

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120 56. (Previously Presented) The integrated circuit package of claim 49 wherein
121 none of the bonding pads are electrically coupled to the transition medium.

122 57. (Previously Presented) The integrated circuit package of claim 49 wherein
123 between the transition medium and the integrated circuit die is only an adhesive layer.

124 58. (Previously Presented) The integrated circuit package of claim 49 wherein
125 the back side of the integrated circuit die faces toward the transition medium.

126 59. (Previously Presented) The integrated circuit package of claim 49 wherein
127 the integrated circuit package is a ball grid array package.

128 60. (Previously Presented) The integrated circuit package of claim 49 wherein
129 the transition medium has a coefficient of thermal expansion between approximately $7 \times 10^{-6}/^{\circ}\text{C}$
130 and $17 \times 10^{-6}/^{\circ}\text{C}$.

131 61. (Previously Presented) The integrated circuit package of claim 49 further
132 comprising:
133 solder balls, below the metallized polymer layer and integrated circuit die,
134 electrically coupled to the bonding pads.

135 62. (Previously Presented) An integrated circuit package comprising:
136 a substrate;
137 a silicon die comprising a thickness;
138 a transition medium positioned between the substrate and the silicon die; and
139 a plastic encapsulant which encapsulates the silicon die and the transition
140 medium,

141 wherein the transition medium comprises a thickness that is greater than the
142 thickness of the silicon die, the transition medium and the plastic encapsulant each comprising a
143 first mold compound, thereby the coefficient of thermal expansion of the transition medium is
144 approximately equal to that of the plastic encapsulant.

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145 63. (Previously Presented) The integrated circuit package of claim 62 wherein
146 a first edge of the transition medium is coincident with a first edge of the silicon die, and a
147 second edge of the transition medium is coincident with a second edge of the silicon die.

148 64. (Previously Presented) The integrated circuit package of claim 62 wherein
149 the distance from the top of the plastic encapsulant to the bottom of the substrate defines a
150 package thickness and the silicon die is positioned at approximately a midpoint of the package
151 thickness.

152 65. (Cancelled)

153 66. (Previously Presented) The integrated circuit package of claim 62 wherein
154 the transition medium has a coefficient of thermal expansion between approximately $7 \times 10^{-6}/^{\circ}\text{C}$
155 and $17 \times 10^{-6}/^{\circ}\text{C}$.

156 67. (Previously Presented) An integrated circuit package comprising:
157 a silicon die having a first thickness;
158 a metallized polymer layer having a first side and a second side;
159 a transition medium disposed between the silicon die and the first side of the
160 metallized polymer layer; and
161 a plastic encapsulant which encapsulates the silicon die and the transition
162 medium, wherein the transition medium has a second thickness, the first thickness is less than the
163 second thickness, the plastic encapsulant and the transition medium each comprising a first mold
164 compound, thereby the coefficient of thermal expansion of the transition medium is
165 approximately equal to that of the plastic encapsulant.

166 68. (Previously Presented) The integrated circuit package of claim 67 wherein
167 the coefficient of thermal expansion of the transition medium is greater than the coefficient of
168 thermal expansion of the silicon die.

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169 69. (Previously Presented) An integrated circuit package capable of being
170 coupled to a printed circuit board comprising:
171 a silicon die having a first thickness;
172 a metallized polymer layer;
173 a transition medium having a second thickness; and
174 a plastic encapsulant which encapsulates the silicon die and the transition
175 medium; and
176 wherein the transition medium is disposed between the silicon die and the
177 metallized polymer layer,
178 wherein the first thickness is less than the second thickness,
179 wherein a first edge of the transition medium is coincident with a first edge of the
180 silicon die,
181 wherein a second edge of the transition medium is coincident with a second edge
182 of the silicon die, and
183 wherein both the transition medium and the plastic encapsulant have a coefficient
184 of thermal expansion less than the coefficient of thermal expansion of the printed circuit board to
185 which the integrated circuit package is capable of being coupled and greater than the coefficient
186 of thermal expansion of the silicon die.

187 70. (previously presented) The integrated circuit package of claim 3 wherein
188 the coefficient of thermal expansion of the transition medium is approximately equal to that of
189 the plastic encapsulant.